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Jameco Part Number 41398

256K x 1 Bit Dynamic RAM with Page/Nibble Mode

FEATURES

- **Performance range**

	t_{RAC}	t_{CAC}	t_{RC}
KM41256/7A-10	100ns	50ns	200ns
KM41256/7A-12	120ns	60ns	230ns
KM41256/7A-15	150ns	75ns	260ns

- **Page Mode capability-KM41256A**
- **Nibble Mode capability-KM41257A**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **$\overline{RAS}$-only and Hidden Refresh capability**
- **TTL compatible inputs and output**
- **Common I/O using early write**
- **Single +5V±10% power supply**
- **256 cycle/4ms refresh**
- **JEDEC standard pinout in 16-pin plastic DIP, 18 lead PLCC and 16-pin plastic ZIP.**

DESCRIPTION

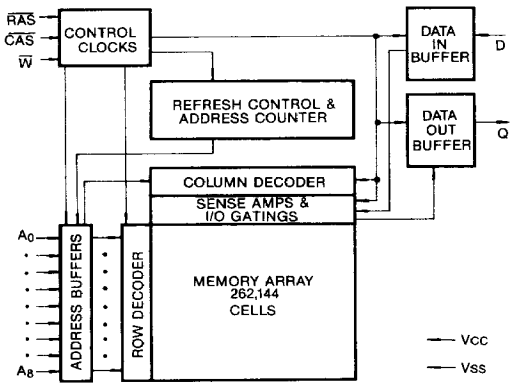
The KM41256/7A is a fully decoded NMOS Dynamic Random Access Memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as computer memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The KM41256A features page mode which allows high speed random access of memory cells within the same row. The KM41257A features nibble mode which allows high speed serial access of up to 4 bits of data. $\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. Multiplexed row and column address inputs permit the KM41256/7A to be housed in a JEDEC standard 16-pin DIP.

The KM41256/7A is fabricated using Samsung's advanced silicon gate NMOS process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size.

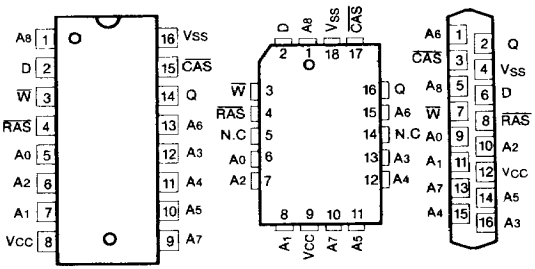
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

- **KM41256/7AP** **•KM41256/7AJ** **•KM41256/7AZ**



Pin Name	Pin Function
A_0-A_8	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

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ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7.0	V
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OS}	50	mA

*Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	−1	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ cycling; @t_{RC} = min.)	KM41256/7A-10	I_{CC1}	—	85	mA
	KM41256/7A-12		—	75	mA
	KM41256/7A-15		—	65	mA
Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		I_{CC2}	—	4.5	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; @t_{RC} = min.)	KM41256/7A-10	I_{CC3}	—	70	mA
	KM41256/7A-12		—	65	mA
	KM41256/7A-15		—	60	mA
Page Mode Current* ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; @t_{PC} = min.)	KM41256A-10	I_{CC4}	—	65	mA
	KM41256A-12		—	55	mA
	KM41256A-15		—	45	mA
Nibble Mode Current* ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; @t_{NC} = min.)	KM41257A-10	I_{CC5}	—	65	mA
	KM41257A-12		—	55	mA
	KM41257A-15		—	45	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ cycling @t_{RC} = min.)	KM41256/7A-10	I_{CC6}	—	70	mA
	KM41256/7A-12		—	65	mA
	KM41256/7A-15		—	60	mA
Input Leakage Current (Any input $0 \le V_{IN} \le 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$, all other pins not under test = 0 volts.)		I_{IL}	−10	10	μA

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DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$)	I_{OL}	−10	10	μA
Output High Voltage Level ($I_{OH} = -5mA$)	V_{OH}	2.4	—	V
Output Low Voltage Level ($I_{OL} = 4.2mA$)	V_{OL}	—	0.4	V

*Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current.

CAPACITANCE ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_8, D)	C_{IN1}	—	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)	C_{IN2}	—	10	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$. See notes 1,2)

KM41256/7A STANDARD OPERATION

Parameter	Symbol	KM41256A-10 KM41257A-10		KM41256A-12 KM41257A-12		KM41256A-15 KM41257A-15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	200		230		260		ns	
Read-modify-write cycle time	t_{RWC}	245		265		310		ns	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	3.4
Access time from $\overline{CAS}$	t_{CAC}		50		60		75	ns	3.5
Output buffer turn-off delay time	t_{OFF}	0	25	0	30	0	40	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	90		100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		ns	
$\overline{CAS}$ precharge time (all cycles except page mode)	t_{CPN}	45		50		60		ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	110		120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	4
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	15		15		15		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	

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KM41256/7A STANDARD OPERATION (Continued)

Parameter	Symbol	KM41256A-10 KM41257A-10		KM41256A-12 KM41257A-12		KM41256A-15 KM41257A-15		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{RAS}$	t_{AR}	65		80		100		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		20		ns	
Write command set-up time	t_{WCS}	0		0		0		ns	7
Write command hold time	t_{WCH}	35		40		45		ns	
Write command pulse width	t_{WP}	35		40		45		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		40		45		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	
Data-in hold time	t_{DH}	35		40		45		ns	
$\overline{CAS}$ to write enable delay time	t_{CWD}	50		60		75		ns	7
$\overline{RAS}$ to write enable delay time	t_{RWD}	100		120		150		ns	7
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		100		120		ns	
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	85		100		120		ns	
Refresh period (256 cycles)	t_{REF}		4		4		4	ms	

KM41256/7A $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	20		25		30		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	50		55		60		ns	
Refresh counter test cycle time	t_{RTC}	330		375		430		ns	
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	50		60		70		ns	
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	230		265		320		ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ hold time	t_{RPC}	20		20		20		ns	

KM41257A NIBBLE MODE

Nibble mode read/write cycle time	t_{NC}	50		60		75		ns	
Nibble mode read-write cycle time	t_{NRWC}	75		90		105		ns	
Nibble mode access time	t_{NCAC}		20		30		40	ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	20		30		40		ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	20		25		30		ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	30		40		50		ns	
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	20		20		20		ns	
Nibble mode $\overline{CAS}$ to $\overline{W}$ delay time	t_{NCWD}	30		30		35		ns	
Nibble mode $\overline{W}$ to $\overline{CAS}$ lead time	t_{NCWL}	25		25		30		ns	

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KM41256A PAGE MODE (Continued)

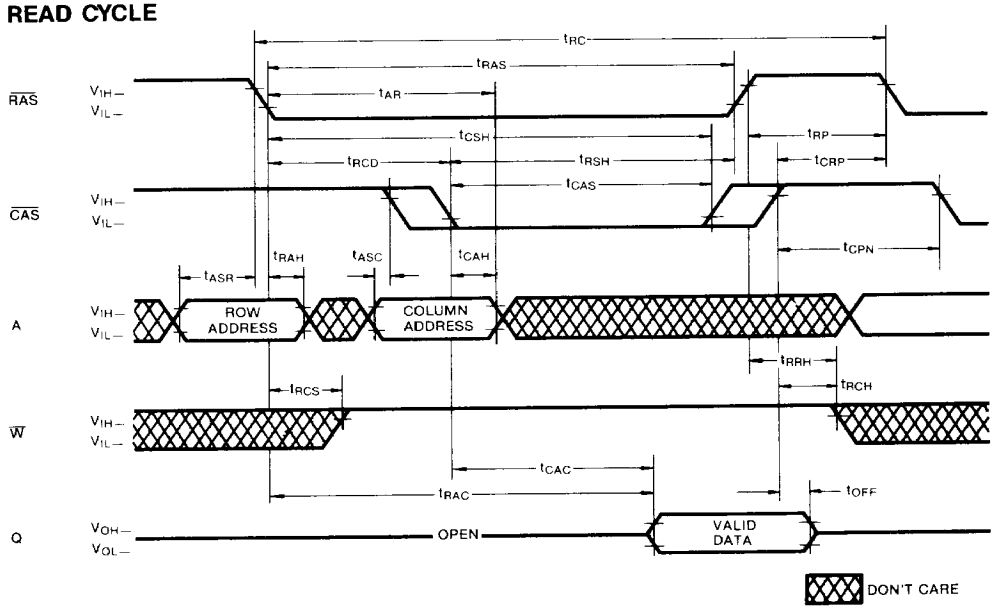
Parameter	Symbol	KM41256A-10		KM41256A-12		KM41256A-15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Page mode cycle time	t_{PC}	100		120		145		ns	
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	45		50		60		ns	

NOTES

1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{CWD} and t_{RWD} are restrictive operating parameters for the read-modify-write cycle only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} > t_{RWD}$(min), the cycle is a late write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

TIMING DIAGRAMS

READ CYCLE



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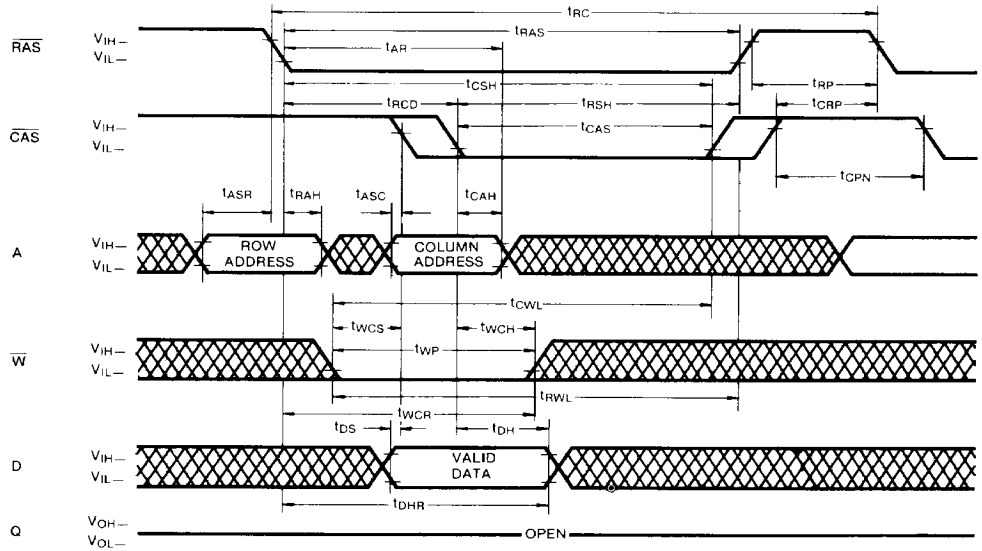
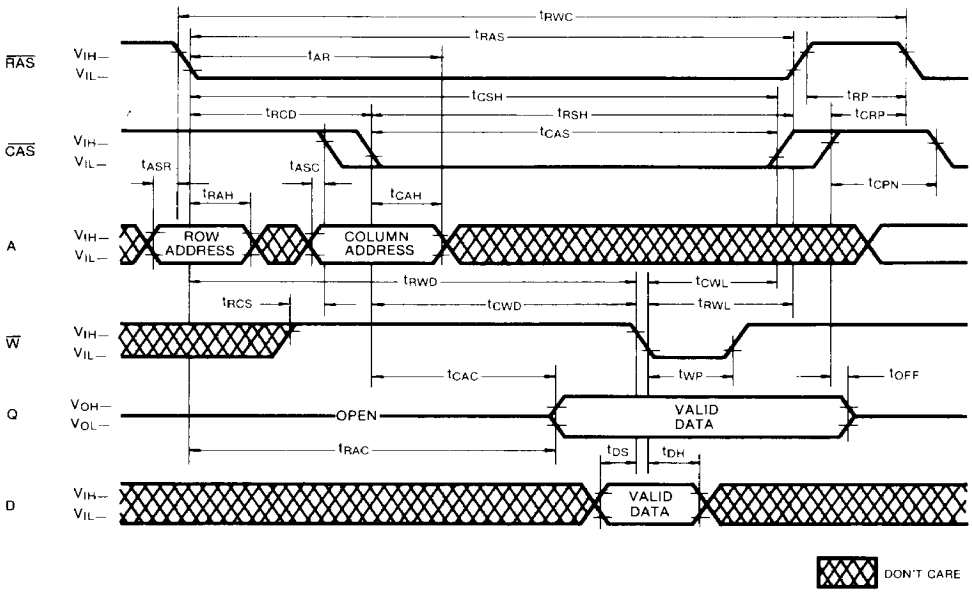
TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



READ-WRITE/READ-MODIFY-WRITE CYCLE



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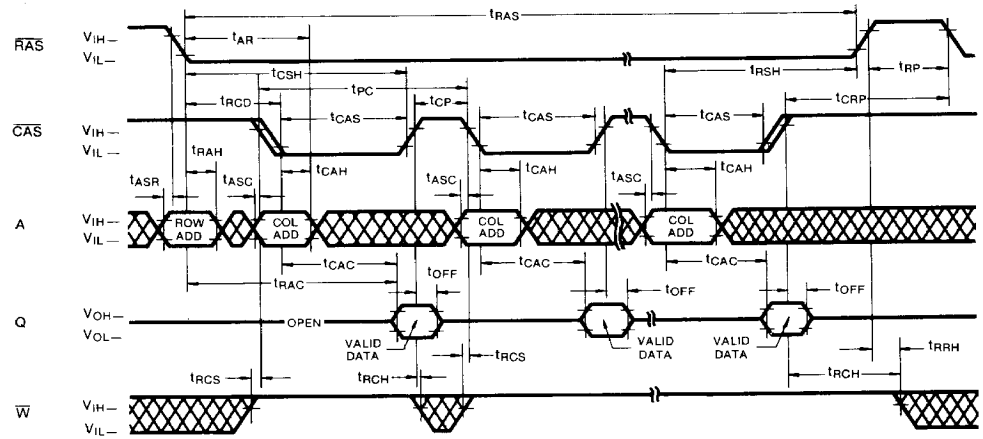
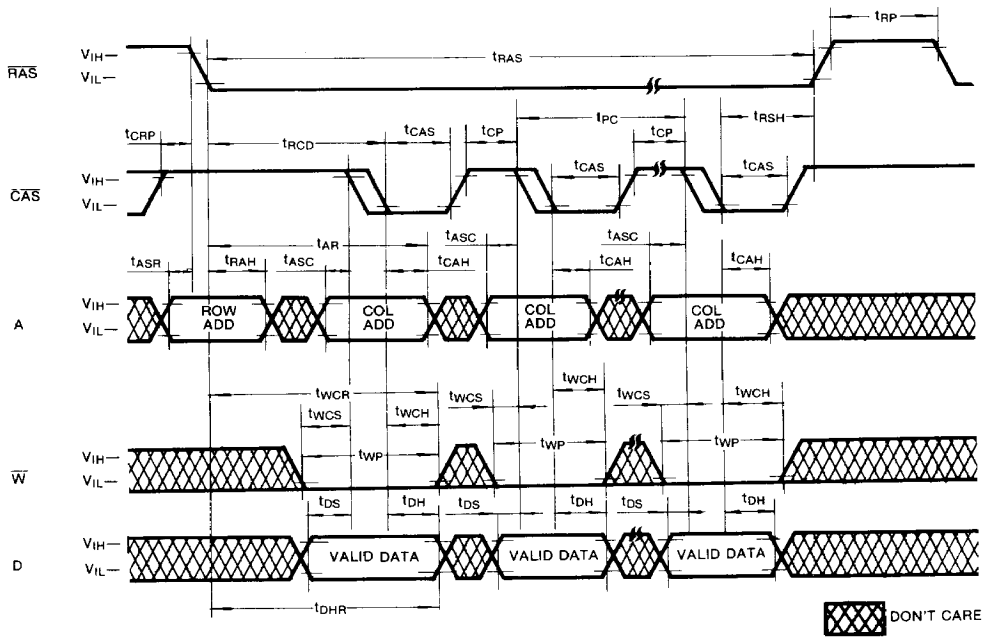
TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE (KM41256A)



PAGE MODE WRITE CYCLE (KM41256A)



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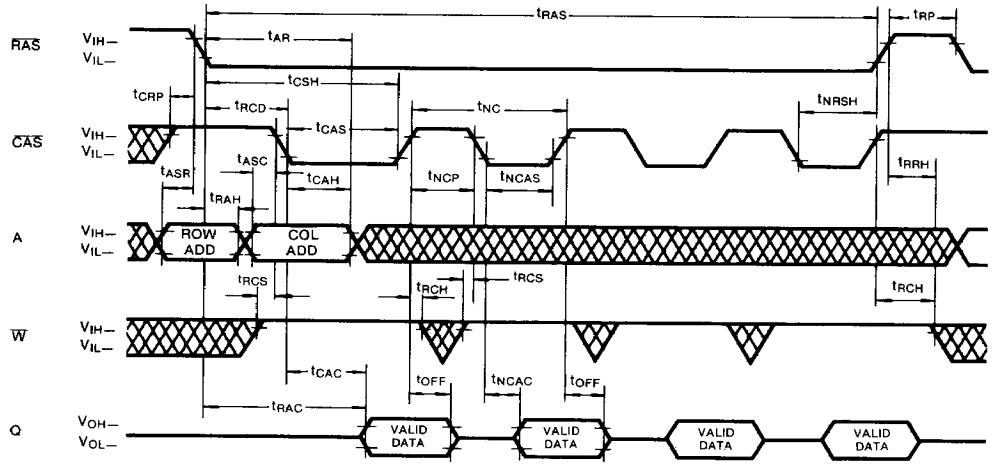
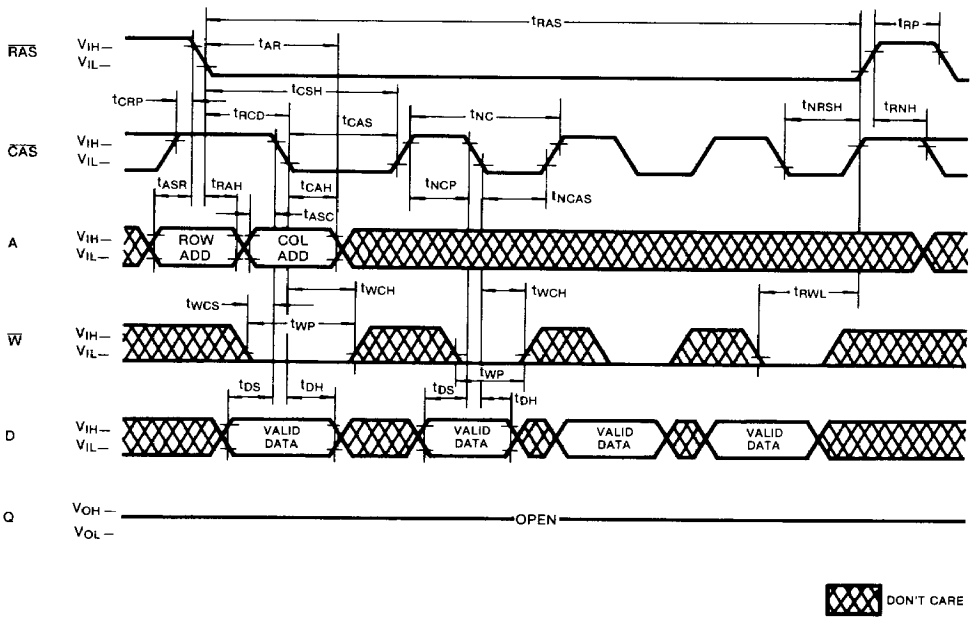
TIMING DIAGRAMS (Continued)

NIBBLE MODE READ CYCLE (KM41257A)



NIBBLE MODE WRITE CYCLE (KM41257A)



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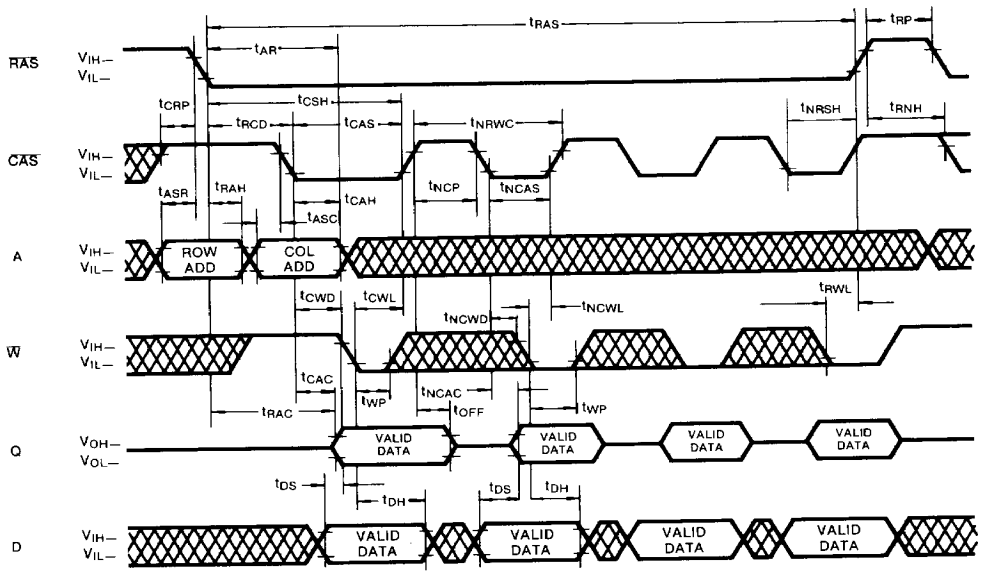
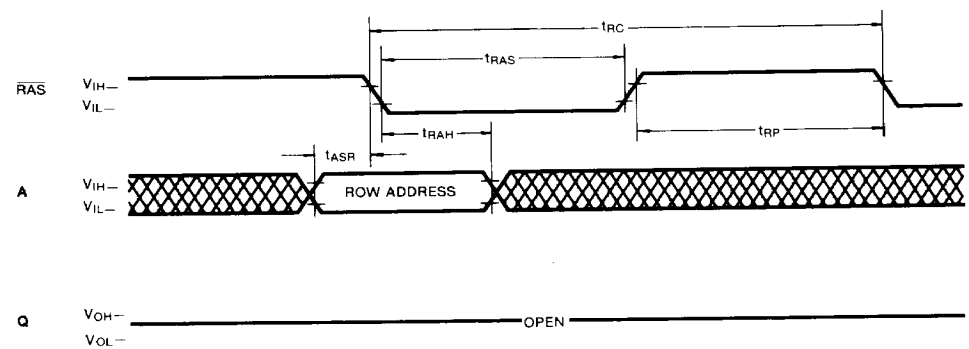
TIMING DIAGRAMS (Continued)

NIBBLE MODE READ-WRITE CYCLE (KM41257A)



RAS-ONLY REFRESH CYCLE

NOTE: CAS = V_{IH}, W, D = Don't Care



DON'T CARE

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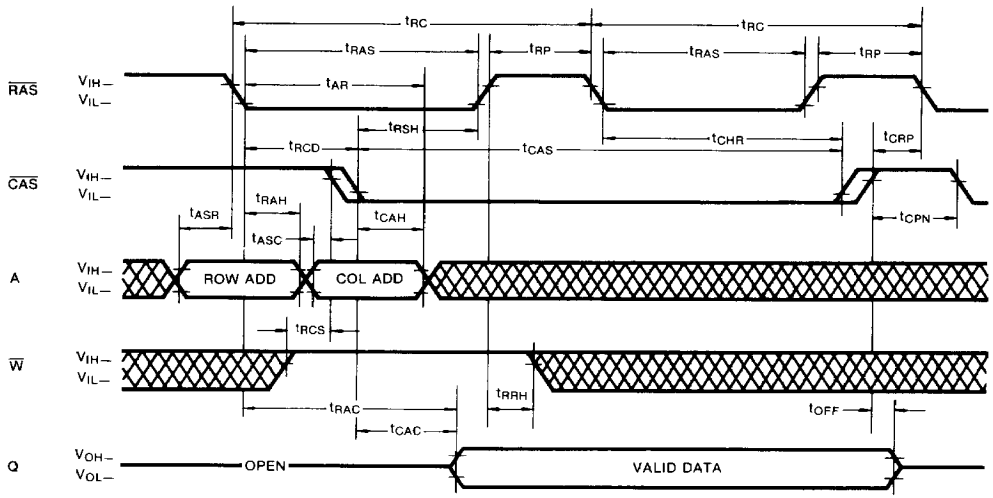
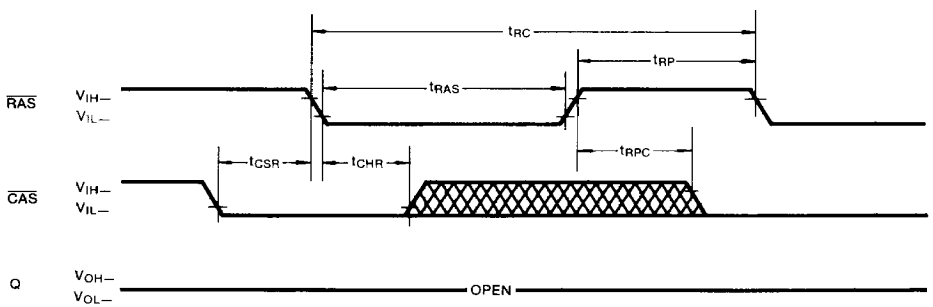
TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH CYCLE

NOTE: Address, W, D = Don't Care



DON'T CARE

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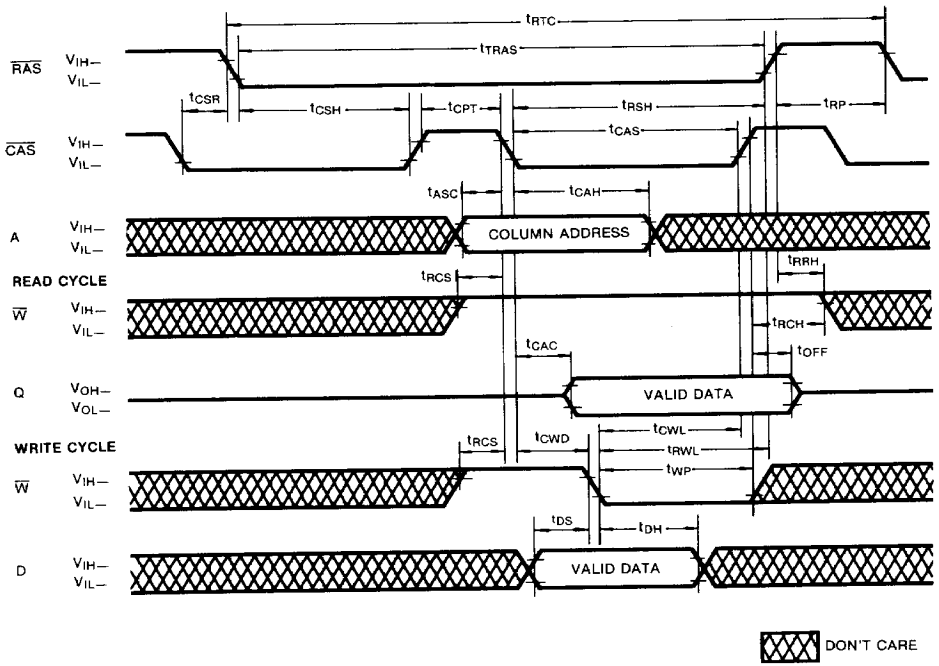
TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



KM41256/7A OPERATION

Device Operation

The KM41256/7A contains 262,144 memory locations. Eighteen address bits are required to address a particular memory location. Since the KM41256/7A has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the KM41256/7A begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any KM41256/7A cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse width are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41256/7A begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

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DEVICE OPERATION (Continued)

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The output of the KM41256/7A remains in the Hi-Z state until valid data appears at the output. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The KM41256/7A can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} and t_{CWD}, are not necessarily met. The state of data-out is indeterminate since the output could be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41256/7A has a three-state output buffer which is controlled by $\overline{CAS}$ (and $\overline{W}$ for early write).

Whenever $\overline{CAS}$ is high (V_{IH}), the output is in the high impedance (Hi-Z) state, In any cycle in which valid data appears at the output, the output first remains in the Hi-Z state until the data is valid and then the valid data appears at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM41256/7A operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Page Mode Read, Page Mode Read-Modify-Write. Nibble Mode Read, Nibble Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Page Mode Write, Nibble Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41256/7A is stored on a tiny capacitor within each memory cell. Due to leakage, the data will leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 4 ms There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM41256/7A has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addressed. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs and the on-chip refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and strobing in a refresh row address with $\overline{RAS}$. The KM41256/7A hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required in hidden refresh cycles by DRAMS that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Other Refresh Methods: It is also possible to refresh the KM41256/7A by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only refresh is the preferred method.

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DEVICE OPERATION (Continued)

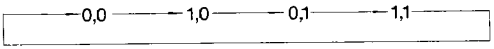
Page Mode (KM41256A)

The KM41256A has page mode capability. Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Nibble Mode (KM41257A)

The KM41257A has nibble mode capability. Nibble mode operation allows high speed serial read, write or read-modify-write access of 4 consecutive bits. The first of 4 bits is accessed in the usual manner. The remaining nibble bits are accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low.

The 4 bits of data that may be accessed during nibble mode are determined by the lower 8 row address bits (RA_0-RA_7) and 8 column address bits (CA_0-CA_7). The two address bits, $RA_8$and CA_8, are used to select 1 of the 4 nibble bits for initial access. The remaining nibble bits are accessed by toggling $\overline{CAS}$ with $\overline{RAS}$ held low. Each high-low $\overline{CAS}$ transition will internally increment the nibble address (RA_8, CA_8) as shown in the following diagram.



If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on a subsequent access, the new data will be written into the selected cell location.

A nibble cycle can be a read, write, or read-modify-write cycle. Any combinations of reads and writes or read-modify-writes are allowed.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter test cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

Row Address—Bits A0 through A7 are supplied by the on-chip refresh counter. The A8 bit is set high internally.

Column Address—Bits A0 through A8 are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedures

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 256 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 256 times so that highs are written into the 256 memory cells.
4. Read the "highs" written during step 3.
5. Compliment the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS}$=V_{SS} during power-up the KM41256/7A might begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 100μsec is required after power-up followed by 8 initialized cycles before proper device operation is assured. Eight initialization cycles are also required after any 4 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41256/7A inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be us-

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DEVICE OPERATION (Continued)

ed, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41256/7A input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling cannot be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). The total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

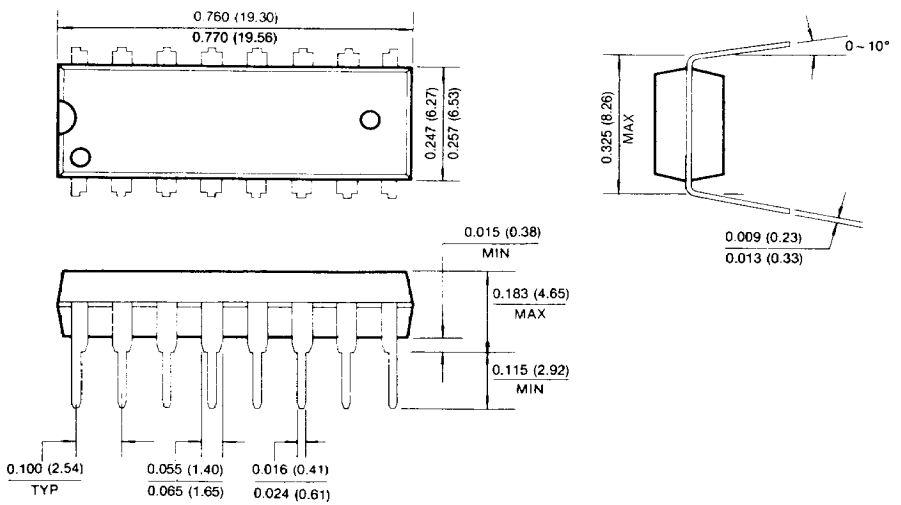
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM41256/7A using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41256/7A and they supply much of the current used by the KM41256/7A during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.3μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor throughout the memory array.

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (millimeters)



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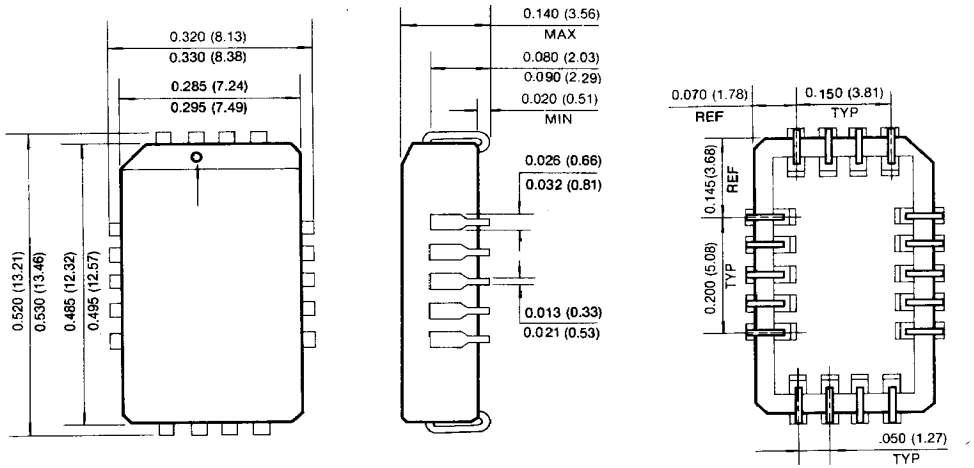
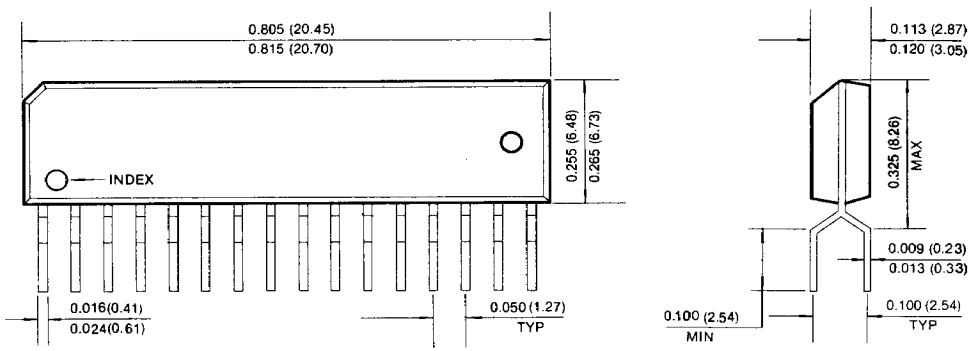
PACKAGE DIMENSIONS (Continued)

18-PIN PLASTIC LEADED CHIP CARRIER

Units: Inches (millimeters)



16-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE



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